

# SUBSTRATE INDEPENDENT MULTIPLE INPUT BI-DIRECTIONAL ESD PROTECTION STRUCTURE

## Field of the Invention

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The invention relates to ESD protection structures. In particular it relates to protection structures capable of protecting two or more inputs against ESD events.

## Background of the Invention

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In dealing with ESD protection several factors invariably impact the choice and structure of the protection structure. Typical factors that need to be considered in providing ESD protection for a circuit, include the triggering and breakdown voltage of the ESD device, its holding voltage, current handling capabilities, and ability to handle positive and negative voltage pulses. These diverse requirements can best be understood by way of example.

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For instance, one common ESD protection structure is the silicon-controlled rectifier (SCR) shown in Figure 1, which includes an n-well 100 formed in a p-substrate 102. A p+ and an n+ region 110, 112 are formed in the n-well and are typically connected to define an anode. A p+ and an n+ region 120, 122 are also formed in the p-substrate 102 to define a cathode. This device provides excellent protection against high current during ESD events. One of the advantages of SCR 100 over other ESD protection devices, such as a grounded-gate MOS transistor, is the double injection of carriers, which provides current densities (after snapback) that are about ten times greater than the densities provided by a grounded-gate MOS device.

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One of the disadvantages of a SCR, however, is that a very large positive voltage, e.g., 50 volts, must be dropped across its nodes before the junction breaks down. As a result, SCRs can not be used to protect devices, such as MOS transistors, that can be permanently damaged by much lower voltages, e.g., 15 volts.

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A solution proposed in the past, was to use low voltage silicon controlled rectifiers (LVTSCRs) which are not only smaller but allow the reaching of current

densities, after snap back, that are some ten times higher than the current densities of traditionally used grounded gate NMOS devices (GGNMOS), thus increasing the ESD protection capability for CMOS circuits.

However conventional LVTSCRs also have their limitations. For instance,  
5 they fail to address yet another concern in designing ESD protection devices, namely the ability to accommodate both positive and negative polarity voltage pulses. Situations present themselves where bi-directional voltage swings need to be handled. One scenario is in the case where the power circuit is working on inductive loads. Here both negative and positive voltage waveforms can be produced. For example, in  
10 order to detect small signals from a power circuit, it is common to make use of differential amplifiers that include inductive loads as shown in Figure 2. The circuit in figure 2 shows a differential amplifier 200 measuring the voltage between two input pads 210, 212. In this circuit, the one input pad 210 is provided with an inductive load 204. To protect the circuit against ESD pulses on either one of the  
15 input pads, an ESD protection circuit 202 is provided. This has to be able to handle both positive and negative voltage pulses on the two input pads.

In the case of high voltage applications, the ESD protection structure has to be able to handle high voltages without triggering. This need for a high voltage solution is becoming particularly acute in the motor vehicle industry where the number of  
20 electronic components is not only increasing but a new high voltage standard of 42V is being promoted.

Furthermore, in order to avoid interference with the circuit signal and ensure good accuracy it is desirable that the input to the analog circuit have no body diode.

It will thus be appreciated that, the diverse requirements are not necessarily  
25 present in one structure, thus requiring that new structures be created.

#### Summary of the Invention:

According to the invention, there is provided a multiple input ESD protection,  
30 comprising a first p-well formed in a first n-well, a second p-well formed in a second

n-well, an isolation ring between the n-wells and extending around the two n-wells, a first input region formed in the first p-well, a second input region formed in the second p-well, a contact to the first input region, a contact to the second input region, and a contact to the isolation ring. For purposes of this application, the term contact  
5 will be used broadly to refer to the means for contacting the input region. Thus it will include both the polysilicon contact region and the metal contact to the polysilicon contact region. For simplicity, the metal layers and metal contact regions are not shown in the embodiments even though they form part of the contact.

The isolation ring can be a p+ region or a combination of a first p+ region, a  
10 n+ region, and a second p+ region formed adjacent to each other and extending around the n-wells. The isolation ring may be formed in a p-well and may have a p-buried layer (PBL) formed below the p-well of the isolation ring.

An n-isolation region (NISO) may be formed beneath one or both of the n-wells. A p-buried layer (PBL) may be formed beneath one or both of the p-wells.

15 One or both of the first and second input regions may include a p+ region and an n+ region. Instead the first input region may include only a p+ region or only a n+ region and the second input region may have both a n+ and a p+ region or only a region of opposite polarity to that of the first input.

Further, according to the invention, there is provided an ESD protection  
20 device that comprises a structure as defined above, wherein the isolation ring is connected to ground or is biased to a predefined voltage.

## 25 Brief Description of the Drawings:

Figure 1 shows a cross section through a typical SCR;

Figure 2 is a simple schematic circuit diagram of a circuit with an inductive load, and

Figures 3-7 show cross sections through five embodiments of ESD protection  
30 structures of the invention.

5     Detailed Description of the Invention:

          The present invention provides a new bi-directional structure and an ESD protection device making use of the structure that provides for positive and negative voltage swings on the input pads. Furthermore, the present invention provides for ESD protection on more than one input pin, and provides for independent operation  
10    relative to the substrate by including substrate isolation. For instance, as will be described in more detail below, an isolation ring is provided to isolate the substrate.

          Figure 3 shows one embodiment of the present invention. The structure 300 comprises a symmetrical structure with two n-wells 302, 304 formed in a p-substrate 306. The n-wells 302, 304 are isolated from the p-substrate by n-isolation regions  
15    (NISO) 312, 314, respectively.

          As shown in Figure 3, the structure supports two poly input contact regions, 320, 322, each of which is connected to a n+ and a p+ input region formed in a p-well. As mentioned above, even though the term contact typically refers to the metal contact, the present application will use the term contact to refer to both the metal  
20    contact (not shown in the embodiments) as well as to the poly contact region. For simplicity, therefore, the poly contact regions shown in the Figures will simply be referred to as contacts. Thus, contact 320 is connected to p+ region 330 and n+ region 332 formed in p-well 340, while contact 322 is connected to p+ region 334 and n+ region 336, which are formed in p-well 342. As shown in Figure 3, p-well 340 is  
25    formed in n-well 302, and p-well 342 is formed in n-well 304. P-well 340 has a p-buried layer (PBL) 350 formed below it while p-well 342 has PBL 352 formed below it. Thus, the structure provides support for two inputs, each of which are connected to a p+ and an n+ input region to handle dual voltage swings. The PBLs 350, 352 provide isolation between the n+ regions 332, 336, and the n-wells 302, 304,  
30    respectively, to avoid punch-through during negative ESD voltage pulses.

The NISOs 312, 314, in turn, provide punch-through isolation between the p+ regions 330, 334 and p-substrate 306 during positive ESD voltage pulses.

It will be noted that the structure of Figure 3 differs from the SCR known in the art, shown in Figure 1, in that the structure of Figure 3 is symmetrical with two n-wells, a p-well in each n-well, and n+ and p+ regions connected to each input, thus  
5 handling both positive and negative ESD voltage pulses.

The embodiment of Figure 3 further includes an isolation ring in the form of a p+ region 360. The p+ region is formed in a p-well 362, with a p-buried layer (PBL) 364 underneath the well 362. As shown in Figure 3, the isolation ring extends  
10 between the n-wells 302, 304 and around them. Therefore, when viewed from the top (not shown), the isolation ring would surround the two n-wells 302, 304. The isolation ring is connected to ground (contact 370) as shown in Figure 3 and serves as a ground connection independent of the two input contacts 320, 322. Thus the structure provides independent operation for both input pads (connected to the  
15 contacts 320, 322) relative to the substrate, and takes into account positive and negative voltage pulses to either of the two pads. An oxide layer 372 extends between the contacts 320, 322, 370.

The Figure 3 embodiment provides snapback characteristics between the two inputs to contacts 320, 322, while the substrate can be grounded or biased at any  
20 desired potential relative to the two inputs. Thus the ESD device making use of the structure shown in Figure 3 can have a grounded or separately biased isolation ring. Thus, this structure is well-suited for applications such as protecting the differential input pins 210, 212 in Figure 2. The isolation ring provides latch-up isolation by reducing injection from the device junction to the internal circuitry. The PBL 364  
25 helps in reducing cross-talk and latch up.

Another embodiment of the invention is shown in Figure 4, which shows a structure similar to that of Figure 3, but instead of only an isolation ring in the form of a p+ region, this embodiment includes an n+ ring in the middle of the p+ ring. Figure 4, as well as Figures 5 and 6 show only the central part of the structure, it being  
30 understood that the isolation ring in each case extends around the two inputs. The

Figure 4 embodiment, in effect, has two p+ isolation rings 400, 402 formed on either side of an n+ ring 404. The rings 400, 402 can be connected to ground by means of a contact 406, as shown. However, other biasing of the contact 406 is also possible as is discussed below. As shown in Figure 4, the p+ rings 400, 402 and n+ ring 404 are  
5 formed in a p-well 408 formed in p-substrate 409. As in the previous embodiment, there are two inputs regions with contacts 410, 412, (other than contact 406). Each input region includes a p+ region and an n+ region (p+ regions 420, 422, and n+ regions 424, 426). The p+ regions 420, 422 and n+ regions 424, 426 are formed in p-wells 430, 432 as shown, with a PBL 440, 442 under each of the p-wells to prevent  
10 punch through during negative voltage pulses, as was discussed above with respect to the Figure 3 embodiment. Also, this embodiment has n-wells 450, 452 with NISO regions 454, 456 formed below the n-wells 450, 452, respectively to provide punch through protection during positive voltage pulses. It will be appreciated that the symmetrical structure of Figure 4 again provides for dual polarity protection, hence  
15 the isolation provided by the PBLs 440, 442, and NISOs 454, 456. An oxide layer 470 is provided between the contacts 406, 410, 412. By including an n+ ring 404 between p-rings 400, 402, the isolation ring defines a thyristor, not only the Zener diode device for the current path from the inputs to ground, which may be a floating ground node. In the Figure 4 embodiment, there is no PBL below the p-well 408 since the isolation  
20 ring in this embodiment is connected to a grounded pad. In an embodiment where it is connected merely to an internal ground node, a PBL is preferably included below the p-well 408 of the isolation ring.

Yet another embodiment of the invention is shown in Figure 5. This embodiment has a structure similar to that in Figure 4, hence, like elements are given  
25 the same reference numerals as in Figure 4. The Figure 5 embodiment (structure 500), however differs from the one in Figure 4 in that the n+ region 426 of Figure 4 is not present in structure 500. Thus the one input region still includes a n+ and a p+ region 420, 424, while the other input region only includes a p+ region 422. Accordingly, contact 512 is smaller than contact 412.

The rest of the structure is essentially the same as in the Figure 4 embodiment. As in the Figure 4 embodiment, the structure 500 has an isolation ring comprising two p+ rings 400, 402, and an n+ ring 404 is formed between the rings 400, 402. The isolation rings 400, 402 are connected to ground by means of a contact 406. As  
5 shown in Figure 5, the p+ rings 400, 402 and n+ ring 404 are formed in a p-well 408, which is formed in p-substrate 409. Other than contact 406, there are two contacts 410, 512, the first of which is connected to a p+ region and an n+ region (p+ regions 420, and n+ regions 424). The latter (contact 512) is connected only to the p+ region 422) The p+ regions 420, 422 and n+ region 424, are formed in p-wells 430, 432 as  
10 shown, with a PBL 440, 442 under each of the p-wells to prevent punch through during negative voltage pulses. It will be appreciated that if the input to contact 512 is not expected to see negative voltages, the PBL 442 is not necessary. Also, this embodiment has n-wells 450, 452 with NISO regions 454, 456 formed below the n-wells 450, 452, respectively to provide punch through protection during positive  
15 voltage pulses. It will be appreciated that only in the case of a positive voltage pulse to the contact 512 will the structure 500 demonstrate SCR behavior. On the other hand, contact 410, which is connected to both a n+ and a p+ region, provides for dual polarity protection. An oxide layer 470 is provided between the contacts 406, 410, 412.

20 Yet another embodiment is shown in Figure 6, which is similar to the Figure 5 embodiment and therefore the same reference numerals have been used for like elements. This embodiment (structure 600) differs from Figure 5 in that the p+ region 420 has been eliminated and the to the n+ region 424 (contact 610) has been reduced in size. The rest of the structure is essentially the same as in the Figure 5 embodiment.  
25 As in the Figure 5 embodiment, the structure 600 has an isolation ring comprising two p+ rings 400, 402. These are typically connected to ground and act as isolation rings. In addition to the p+ isolation rings there is an n+ ring 404. The isolation rings 400, 402 are connected to ground by means of a contact 406. As shown in Figure 6, the p+ isolation rings 400, 402 and n+ ring 404 are formed in a p-well 408, which is formed  
30 in p-substrate 409. Other than contact 406, there are two contacts 610, 512, the first

of which is connected to a n+ region (n+ regions 424). The latter (contact 512) is connected to a p+ region 422). The n+ region 424 and p+ region 422, are formed in p-wells 430, 432 as shown, with a PBL 440, 442 under each of the p-wells to prevent punch through during negative voltage pulses.

5        Also, this embodiment has n-wells 450, 452 with NISO regions 454, 456 formed below the n-wells 450, 452, respectively to provide punch through protection during positive voltage pulses. It will be appreciated that only in the case of a positive voltage pulse to the contact 512 and a negative voltage pulse to the contact 610 will the structure 600 demonstrate SCR behavior. An oxide layer 470 is provided between  
10       the contacts 406, 410, 412.

         The nature of the architecture of the present invention provides for an added advantage. By making use of a simple structure requiring only a single poly contact layer and metal contact layer for the anode, cathode and isolation ring, a space saving can be achieved by placing the entire structure under the bond pad. Each pad  
15       is approximately 100 $\mu$ m $\times$ 100 $\mu$ m in area, and by using the simple architecture described above, bonding and probing will typically not damage the polysilicon contact layer, thus allowing the entire structure to be formed under a bond pad.

         In yet another embodiment, some space saving is achieved by eliminating the separate isolation ring. Typically the isolation ring and spacings between the active or  
20       input regions (cathode or anode) and the ring are rather large, e.g. 3, 5, and 10 $\mu$ m and even larger. Where the isolation ring extends around both the active regions (which will be referred to also as anode and cathode in this application) as in the Figure 3 embodiment, this can represent a substantial use of space. Where one of the active regions (either the anode or the cathode) is grounded, a space saving can be achieved  
25       by providing the grounded anode or cathode in the form of a ring or partial ring that extends fully or partially around the other active region. Thus, the ring-shaped active region can itself serve as the isolation ring to reduce latch-up. This avoids the need for a separate isolation ring. Such an embodiment is shown in Figure 7 where the cathode 700 forms an isolation ring around anode 702. For ease of illustration, the  
30       same reference numerals were used for like structures as in Figure 5.



While specific embodiments have been described above, it will be appreciated that variations can be adopted without departing from the scope of the invention as defined by the claims. For instance, where an input only includes a n+ region, no NISO is needed to prevent punch through of positive voltage pulses. Similarly, where the input only includes a p+ region, no protection against negative punch through is needed. Hence, no PBL is needed under the p-well in which the p+ region is formed. It will, for instance, be appreciated that an embodiment could have a n+ and a p+ region for one input and only a n+ region for the other input.

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